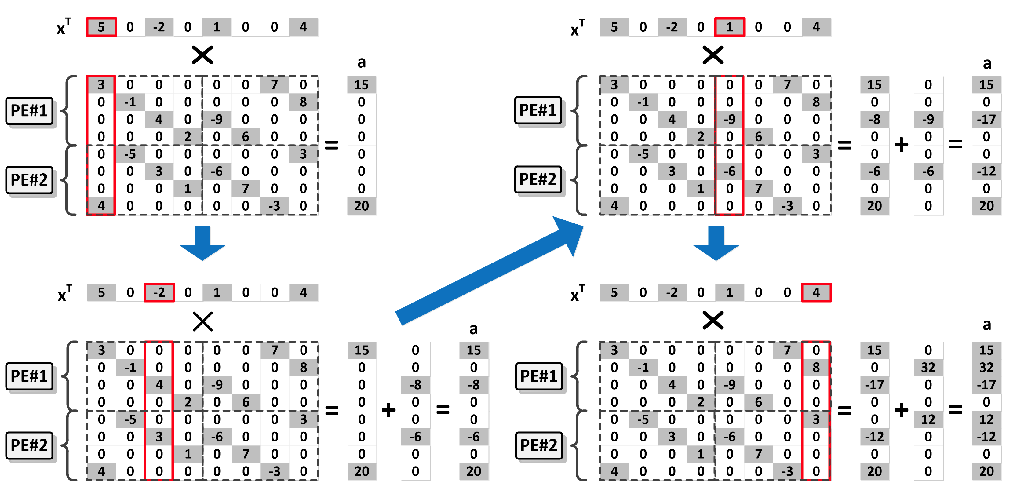
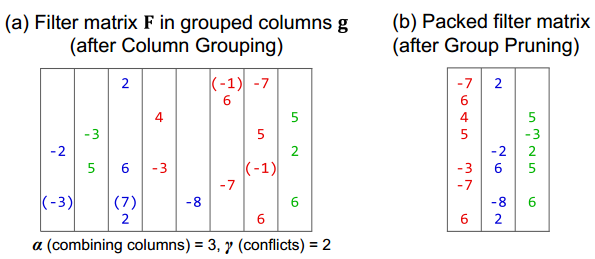
1. Read paper about adding regularity to sparse weight matrix for better hardware implementation:
   1. PERMDNN:

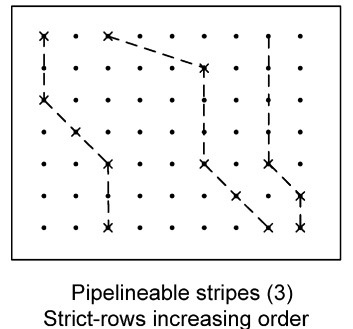


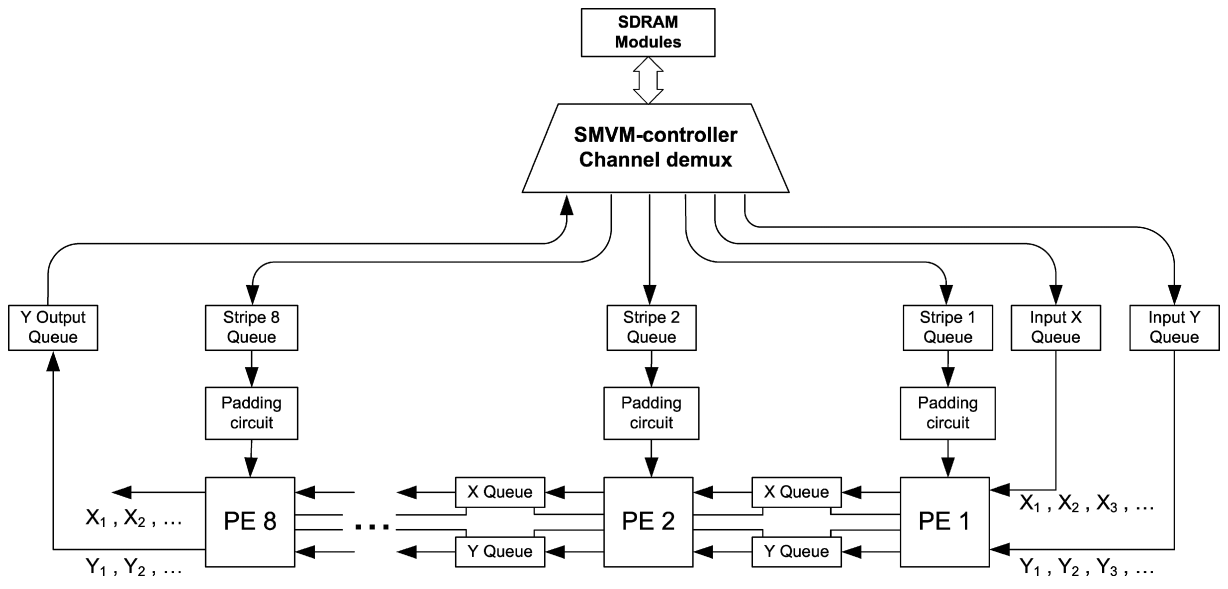
* 1. Column combination:



1. Read paper about storage format of sparse matrix and hardware implementation for SpMV:
   1. COO, CSR, CSC, ELL, DIA
   2. “A Scalable Sparse Matrix-Vector Multiplication Kernel for Energy-Efficient Sparse-Blas on FPGAs”
   3. “FPGA architecture and implementation of sparse matrix–vector

multiplication for the finite element method”:





1. Some thoughts:
   1. Store weights in the format of Booth code
   2. Find another type of regular matrix as the aim of training or design a systolic architecture that can handle sparse matrix with high efficiency
   3. Make use of the overlapping data in matrix of input feature map
   4. Think the data format transform between two adjacent layers